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GB1430007

Publication Title:

GAMING APPARATUS

Abstract:

Abstract of GB1430007

1430007 Indoor games NSM-APPARTEBAU GmbH KG 27 June 1973 [30 June 1972] 30661/73 Heading A6H In a gaming machine, a plurality of indicators are driven either by individual stepping motors or by a common motor and associated friction clutches under the control of a random number generator and are brought to a halt in positions thus randomly determined. These positions are monitored by photo-transistors and are signalled, by way of a position counter and circuitry including coders and decoders, to a circuit matrix pre-programmed with winning combinations, whereby coincidence between the position signals and a particular combination results in the pay out of a prize. Suitable circuit arrangements are described with reference to Figs. 1 and 2 (not shown). Data supplied from the esp@cenet database - Worldwide

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PATENT SPECIFICATION (11) 1 430 007

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(54) IMPROVEMENTS IN GAMING APPARATUS

(71) We, NSM-APPARATEBAU GMBH KOMMANDITGESELLSCHAFT, of 51 Alzeyer Strasse, Bingen, Rhein, Federal Republic of Germany; a German company do hereby declare the invention, for which we pray that a patent may be granted to us, and the method by which it is to be performed, to be particularly described in and by the following statement: —

The present invention concerns an apparatus for producing and identifying winning combinations for a gaming apparatus offering a prize and comprising a random number generator for producing chance dependent operating pulses.

In conventional coin-operated gaming apparatus the random number generator or the dicing mechanism determines the switching off moment and, consequently, a definite position for each of the indicator means carrying a plurality of game symbols. The position of each indicator means is scanned and may thus provide a winning combination. Such a method of scanning by way of scanning levers and locking discs is complicated to manufacture and involves considerable attrition of the individual parts. In addition, the mechanical contacts used in such a method of scanning lead to a relatively high fault liability. Furthermore, the sequential course of the individual steps of the method involves a relatively great deal of time i.e., the random number generator determines the stopping moment of the individual indicator means and then the possible winning combination is determined by scanning.

The object of the present invention is to provide an apparatus of the above type which is as simple and as efficient as possible.

According to the present invention there is provided apparatus for producing and identifying winning combinations for a gaming apparatus, comprising a random number generator for producing random operating pulses for determining the positions of a plurality of indicator means of the gaming apparatus and for providing a count, on a position counter corresponding to the positions of the indicator means, a pre-programmed matrix connected to the counter via an encoder and a decoder, for identifying whether there is a winning combination associated with the count corresponding to the positions of the indicator means.

Preferably, each indicator means has a zero position indicator and an associated photo-transistor detector which photo-transistor is connected to a position counter via an AND gate coupled to a stop phase (DC1, DC2, DC3, DC4 stop) and a common OR gate; each indicator means being driven by a stepping motor adapted to be controlled by a control signal (DC10, DC20, DC30, DC40) which is formed by linking the signal for driving each individual stepping motor during its predetermined operating time and the signal for driving the individual stepping motor during its operating time, determined by the random number generator, and a signal dependent on the value of the random number is coupled to the position counter the output of which is connected to address registers which are associated with the individual indicator means, and are attached via code converters and 1 out of 16 decoders to the programmed matrix.

Further preferably, each indicator means is driven by a common motor via friction clutches, each indicator means being coupled with zero position indicator with an associated photo-transistor the output of which photo-transistor is connected to an AND gate having another input from a stop phase (DC1 stop, DC2 stop, DC3 stop, DC4 stop) the AND gate is coupled via a common OR gate to a position counter further-

more each indicator means being coupled with a position indicator for each position of the indicator means and having an associated photo-transistor the output of which is connected to an AND gate which has another input from the stop phase (DC1 stop, DC2 stop, DC3 stop, DC4 stop) is then connected via a common OR gate to an associated AND gate, the other input of which is the random-dependent signal (RNC) input, to the position counter, the position counter is connected to the 5 Bit address registers associated with the individual indicator means, said registers being connected via bi-stable multi vibrators and corresponding AND gates and inverters to control signals (DC10, DC20, DC30, DC40) which are formed by linking the signals for driving the individual indicator means during the predetermined operating time and the signals for driving the individual indicator means during the operating time determined by the random number generator and the 5 Bit address registers are connected to a programmed matrix by way of code convertors and 1 out of 16 decoders.

The advantages achieved in accordance with the present invention reside more particularly in the feature that the circuit is flexible and, due to its design, not limited in the number of winning combinations. In addition it has no mechanical contacts thus ensuring a high degree of reliability and, moreover, it can serve equally well as the starting point for a remote indicating system. The apparatus itself is simple and operates within a very short period, i.e., the entire process is electronic, the indicator means carrying a plurality of game symbols only fulfilling the function of an indicating unit.

The present invention will be described further, by way of example, with reference to the accompanying drawings, in which:—

Fig. 1 shows a first embodiment of a circuit for carrying out the method of the present invention in which the individual indicator means are each driven by a stepping motor; and

Fig. 2 shows a second embodiment of a circuit according to the invention, in which the indicator means are driven by means of a common motor.

According to Fig. 1, a photo transistor 2 having an attached amplifier 3, is associated with an indicator means 1. A zero position indicator 4 is present on the indicator means 1 so that the zero position can be scanned by the photo transistor 2. The driving motor for the indicator means 1 is a stepping motor 5 driven by pulses 6 from a pulse generator (not shown), via the OR gate 7 and the amplifier 8. The OR gate 7 is open as long as a control signal DC10 is present at the OR gate 7 via an inverter 9. The control signal DC10 is produced by a circuit (not shown) which provides a drive signal for each individual stepping motor, this drive signal for the stepping motor is connected during a predetermined operating time determined by the random number generator. At the end of the operating time, predetermined by the gaming system, a stop phase is produced which can be initiated either manually or automatically. The signal DC1 Stop opens the AND gate 10, so that the signal from the zero position indicator 4, detected by the photo-transistor 2 and amplifier 3, and filtered by the action of the filter stage 11 then resets the position counter 13 through the reset input 14 via the OR gate 12. Thus the position counter 13 operates synchronously with the indicator means 1. During the time in which the random number is not equal to zero, a number is fed into the position counter 13 and this corresponds to the position of the indicator means 1. If the externally produced random number is equal to zero, then a random-dependent signal RNC equals 1 and the control signal DC10 becomes 0, thus the stepping motor 5 is braked at that moment. The signal RNC ensures that no further signal passes through the AND gate 16, to the position counter 13. Thus the number in the position counter corresponds to the position of the indicator means 1 related to the zero position. By means of the negative going edge of the DC10 signal, the bistable multi-vibrator 17 is set so that a "1" appears at its output 18 and opens the AND gate 19, whereby the contents of the position counter 13 are fed into a 5 Bit address register 20. The bistable multi-vibrator is then reset by an externally produced reset operating signal γ so that a "0" appears at its output 18, whereby the AND gate 19 is blocked, and the address register 20 is switched to cyclic operation via the inverter 21. The slide command is given to the position counter 13 and the 5 Bit address register 20 by the clock signal ϕ_1/ϕ_2. The outputs of the 5 Bit address register 20 are connected to a code converter 22. In the code converter 22 the 5 Bit signal is changed to a 4 Bit signal. The outputs of the code converter 22 lead to a 1 out of 16 decoder 23. The outputs of the 1 of 16 decoder 23 are coupled in a matrix 24 to prize outputs 25.

The above-described cycle of the indicator means 1 is repeated with the other indicator means 26, 27, 28. Associated with the indicator means 26 are the photo-transistor 29, the amplifier 30 and the AND gate 31, associated with the indicator means 27 are the photo transistor 32, the amplifier 33 and the AND gate 34, and associated with the indicator means 28 are the photo-transistor 35, the amplifier 36 and the AND gate

37. The AND gates 31, 34, 37 are connected to the filter stage 11. The third input of the AND gates 31, 34, 37 is the particular phase DC2 stop, DC3 stop or DC4 stop associated with the indicator means 26, 27 and 28 respectively. According to which indicator means 26, 27, 28 is now stopped, the position counter 13 is reset via the corresponding AND gate 31, 34, 37 and the OR gate 12 via the reset input 14.

If this resetting of the position counter 13 is effected for example on account of the initiation of the phase DC2 stop, then dependent on the random number a control signal DC20 through the inverter 38 and the OR gate 39 is blocked, and the stepping motor 41 previously running with the pulse 6 by way of the amplifier 40 is stopped. A number corresponding to the position of the indicator means 26 is fed to the position counter 13 by means of the pulse 6 through the AND gate 16 synchronously with the position of the indicator means 26. This operation is completed when the signal DC20 is zero and the signal RNC is 1. The bistable multivibrator 42 is now set by the negative-going edge of the signal DC20 so that its output 43 becomes "1". Thus the AND gate 44 is opened for feeding the contents of the position counter 13 into the 5 Bit address register 45. Recording in the 5 Bit address is effected by means of the clock signal ϕ_1/ϕ_2. After the contents of the position counter 13 are recorded in the 5 Bit address register 45, the bistable multivibrator 42 is reset by the external reset signal γ so that the AND gate 44 is closed and the 5 Bit address register 45 is switched to cyclic operation by way of the inverter 46. A code converter 45 with a 1 out of 16 decoder 48 is associated with this 5 Bit address register 45. The signal decoded through these stages is fed into the matrix 24.

If, therefore, the indicator means 27 or 28, for example is stopped because of the phase DC3—stop or the phase DC4 stop, the preceding operation is repeated by means of the circuit consisting of the components 49, 50, 51, 52, 53, 54, 55, 56, 57, 58 or by means of the circuit consisting of the components 59, 60, 61, 62, 63, 64, 65, 66, 67, 68.

The signals at the outputs of the decoders 23, 48, 58, 68 are combined in the matrix 24 into definite combinations so that output signals appear at one or more of the outputs 25, some of which outputs are associated with the award of a prize.

The indicator means of the embodiment according to Fig. 2 are driven by a common motor. The motor drives an intermediate gear by way of two circular belts the driving force is then transmitted to three driving wheels by way of a toothed-belt. The driving wheels are the driving parts of the friction clutches for the drive of the indicator means. The components used in this embodiment, which correspond to those already described, have the same reference numerals. The indicator means 69 comprises, apart from the zero position indicator 4, also a position indicator 73 for each possible position of the indicator means. If, for example, the phase DC1 stop is initiated by an external circuit, then a signal, filtered by means of the filter stage 11, is fed through the AND gate 10 and the OR gate 12 to the return input 14 of the position counter 13 from the photo-transistor 2 and the amplifier 3. At the same time the AND gate 74 opens for the signals from the photo-transistor 75 scanning the position indicators 73 and conducted through the amplifier 76. The output of the AND gate 74 leads through the OR gate 77 to the AND gate 16. The signal RNC opens, by way of the inverter 15, the AND gate 16 for the signals coming from the OR gate 77 until the externally produced random number is equal to zero, and the signal RNC is equal to one, and the signal DC10 is equal to zero. Thus by means of the signal DC10 and a circuit (not shown), the indicator means 69 is stopped. The content of the position counter 13 now corresponds to the position of the indicator means 69 relative to the zero position. The bistable multivibrator 17 is now set by the negative going edge of the signal DC10 so that a one appears at its output 18 which opens the AND gate 19, whereby the content of the position counter 13 is fed into the 5 Bit address register 20. After this operation the bistable multivibrator 17 is reset by an externally produced operating signal γ so that a zero appears at its output 18, whereby the AND gate 19 is blocked and the 5 Bit address register 20 is controlled for cyclic operation by way of the inverter 21. The shift command is passed to the position counter 13 and the 5 Bit address register 20 by the clock signal ϕ_1/ϕ_2. The 5 Bit address register 20 is connected by its output to a code converter 22. In the code converter 22 the 5 Bit signal is converted to a 4 Bit signal. The outputs of the code converter 22 lead to a 1 out of 16 decoder 23. The outputs of the 1 out of 16 decoder 23 are joined to form prize outputs 25 in a prize matrix 24.

The above described cycle of the indicator means 69 is repeated with the other indicator means 70, 71, 72. Associated with the indicator means 70 is the photo-transistor 29, the amplifier 30 and the gate 31; associated with the indicator means 71 is the photo-transistor 32, the amplifier 33 and the AND gate 34 and associated with the

indicator means 72 is the photo-transistor 35, the amplifier 36 and the AND gate 37. Furthermore, the indicator means 70 is connected via the photo-transistor 78, the amplifier 84 and the AND gate 81, the indicator means 71 is connected via the photo-transistor 79 the amplifier 85 and the AND gate 82, and the indicator means 72 is connected via the photo-transistor 80, the amplifier 86 and the AND gate 83 to the OR gate 77.

The AND gates 31, 34, 37 are coupled to the filter stage 11. The third input of the AND gates 31, 34, 37 and the second inputs of the AND gates 81, 82, 83 are the particular phase DC2 stop, DC3 stop and DC4 stop associated with the respective indicator means 70, 71, 72. According to which indicator means 70, 71, 72, is now stopped, the position counter 13 is reset via the corresponding AND gate 31, 34, 37 and the OR gate 12 via the return input 14. The process is continued according to that of the preceding embodiment so that, in turn, the signals on the outputs of the decoders 23, 48, 58, 68 are combined in the matrix 24 into definite combinations, whereby, if desired, one or more prize outputs 25 are actuated.

The two photo-transistors associated with the particular indicator means are preferably replaced functionally by a single photo-transistor, due to the fact that a predetermined length may be given to the position pulses and a length differing from this length may be given to the zero position, and the particular position may then be obtained from the time ratio of these pulses to each other by means of a cnventional gate circuit.

The circuits are preferably designed in the MOS integrated circuit technique.

WHAT WE CLAIM IS:—

1. Apparatus for producing and identifying winning combinations for a gaming apparatus, comprising a random number generator for producing random operating pulses for determining the positions of a plurality of indicator means of the gaming apparatus and for providing a count, on a position counter corresponding to the positions of the indicator means, a preprogrammed matrix connected to the counter via an encoder and a decoder, for identifying whether there is a winning combination associated with the count corresponding to the positions of the indicator means.

2. Apparatus as claimed in claim 1 in which each indicator means has a zero position indicator and an associated photo-transistor detector, which photo-transistors are connected to the position counter via a respective AND gate controlled by a respective stop phase, and a common OR gate; each indicator means being driven by a stepping motor controlled by a control signal which connects a drive signal for driving each individual stepping motor during a predetermined operating time determined by the random number generator, and a signal dependent on the value of the random number is coupled to the position counter the output of which is connected to address registers which are associated with the individual indicator means and are attached via code convertors and 1 out of 16 decoders to the programmed matrix.

3. Apparatus as claimed in claim 2, in which each stepping motor is driven by means of a common pulse via an OR gate and an amplifier.

4. Apparatus as claimed in claims 2 and 3 in which each OR gate is connected by an inverter to each control signal input.

5. Apparatus as claimed in claims 2-4, in which the random-dependent signal is connected by an inverter and an AND gate to the position counter.

6. Apparatus as claimed in any one of claims 2-5, in which the position counter is connected by way of AND gates to 5 Bit address registers each AND gate having an input from a bi-stable multi-vibrator the state of which is determined by the control signal input and an external operating signal input, and an inverter is interposed in a connection between the bi-stable multi-vibrators and the 5 Bit address registers.

7. Apparatus as claimed in claim 1 in which each indicator means is driven by a common motor via friction clutches, each indicator means having a zero position indicator with an associated photo-transistor the output of which photo-transistor is connected to one input of an AND gate, another input coming from a stop phase, the AND gate is coupled via a common OR gate to the position counter, furthermore, each indicator means has a position indicator for each position of the indicator means and has an associated photo-transistor the output of which is connected to an AND gate which has another input from the stop phase and is then connected via a common OR gate to an associated AND gate, the other input of which is a random-dependent signal input, to the position counter, the position counter is connected to the 5 Bit address registers associated with the individual indicator means, said registers being connected to respective bi-stable multi-vibrators, AND gates and inverters, controlled by control signals which also control the connection of the signals for driving the individual indicator means during the predetermined operating time determined by the random number generator and the 5 Bit address registers are connected to a programmed

matrix by way of code converters and 1 out 16 decoders.

8. Apparatus as claimed in claims 2-7, in which the circuit is designed as an integrated circuit.

9. Apparatus for producing and identifying winning combinations for a gaming apparatus substantially as herein described with reference to and as illustrated in Fig. 1 of the accompanying drawings.

10. Apparatus for producing and identifying winning combinations for a gaming apparatus substantially as herein described with reference to and as illustrated in Fig. 2 of the accompanying drawings.

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1430007 COMPLETE SPECIFICATION

2 SHEETS *This drawing is a reproduction of the Original on a reduced scale*

Sheet 1

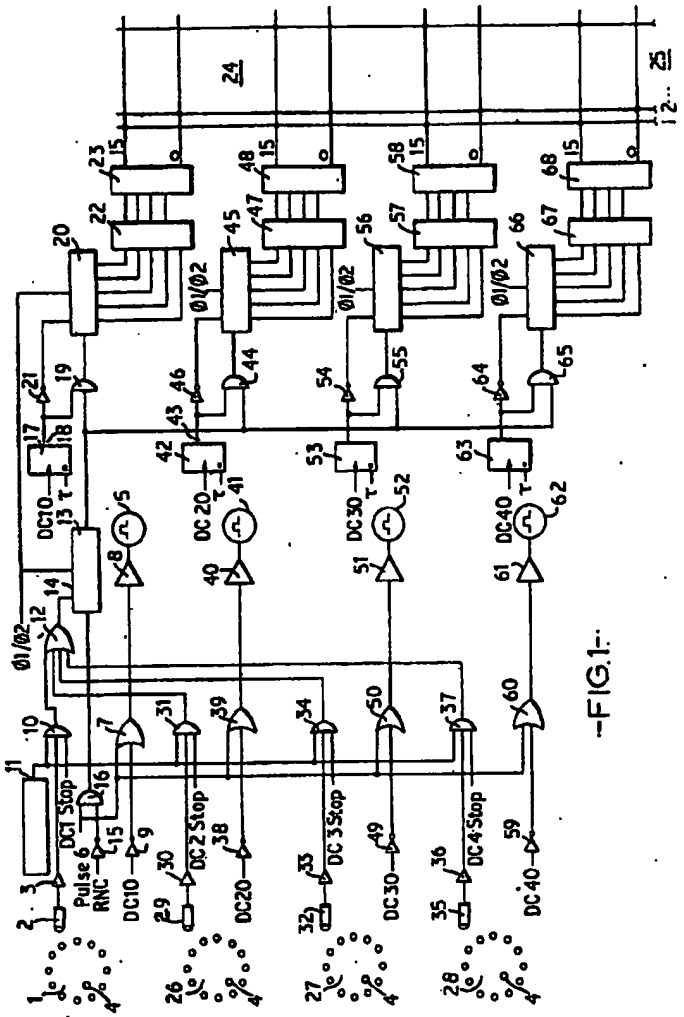

FIG.1.

1430007 COMPLETE SPECIFICATION
2 SHEETS This drawing is a reproduction of the Original on a reduced scale
Sheet 2

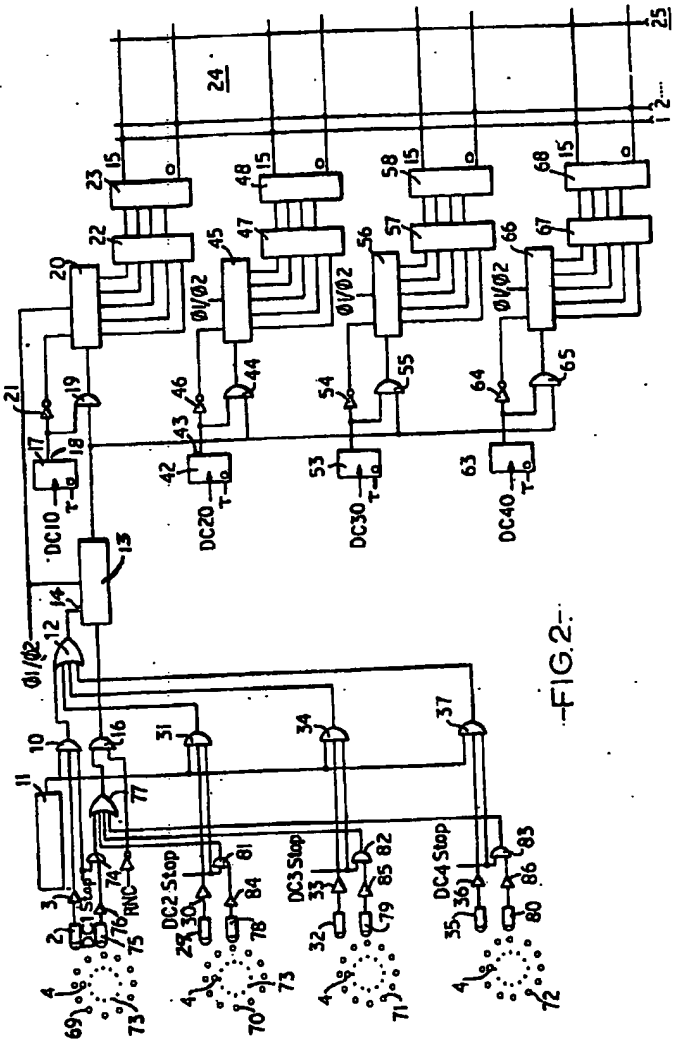

FIG.2.

GB1430007

Publication Title:

GAMING APPARATUS

Abstract:

Abstract of GB1430007

1430007 Indoor games NSM-APPARTEBAU GmbH KG 27 June 1973 [30 June 1972] 30661/73 Heading A6H In a gaming machine, a plurality of indicators are driven either by individual stepping motors or by a common motor and associated friction clutches under the control of a random number generator and are brought to a halt in positions thus randomly determined. These positions are monitored by photo-transistors and are signalled, by way of a position counter and circuitry including coders and decoders, to a circuit matrix pre-programmed with winning combinations, whereby coincidence between the position signals and a particular combination results in the pay out of a prize. Suitable circuit arrangements are described with reference to Figs. 1 and 2 (not shown). Data supplied from the esp@cenet database - Worldwide

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The present invention concerns an apparatus for producing and identifying winning combinations for a gaming apparatus offering a prize and comprising a random number generator for producing chance dependent operating pulses.

In conventional coin-operated gaming apparatus the random number generator or the dicing mechanism determines the switching off moment and, consequently, a definite position for each of the indicator means carrying a plurality of game symbols. The position of each indicator means is scanned and may thus provide a winning combination. Such a method of scanning by way of scanning levers and locking discs is complicated to manufacture and involves considerable attrition of the individual parts. In addition, the mechanical contacts used in such a method of scanning lead to a relatively high fault liability. Furthermore, the sequential course of the individual steps of the method involves a relatively great deal of time i.e., the random number generator determines the stopping moment of the individual indicator means and then the possible winning combination is determined by scanning.

The object of the present invention is to provide an apparatus of the above type which is as simple and as efficient as possible.

According to the present invention there is provided apparatus for producing and identifying winning combinations for a gaming apparatus, comprising a random number generator for producing random operating pulses for determining the positions of a plurality of indicator means of the gaming apparatus and for providing a count, on a position counter corresponding to the positions of the indicator means, a pre-programmed matrix connected to the counter via an encoder and a decoder, for identifying whether there is a winning combination associated with the count corresponding to the positions of the indicator means.

Preferably, each indicator means has a zero position indicator and an associated photo-transistor detector which photo-transistor is connected to a position counter via an AND gate coupled to a stop phase (DC1, DC2, DC3, DC4 stop) and a common OR gate; each indicator means being driven by a stepping motor adapted to be controlled by a control signal (DC10, DC20, DC30, DC40) which is formed by linking the signal for driving each individual stepping motor during its predetermined operating time and the signal for driving the individual stepping motor during its operating time, determined by the random number generator, and a signal dependent on the value of the random number is coupled to the position counter the output of which is connected to address registers which are associated with the individual indicator means, and are attached via code converters and 1 out of 16 decoders to the programmed matrix.

Further preferably, each indicator means is driven by a common motor via friction clutches, each indicator means being coupled with zero position indicator with an associated photo-transistor the output of which photo-transistor is connected to an AND gate having another input from a stop phase (DC1 stop, DC2 stop, DC3 stop, DC4 stop) the AND gate is coupled via a common OR gate to a position counter further-

more each indicator means being coupled with a position indicator for each position of the indicator means and having an associated photo-transistor the output of which is connected to an AND gate which has another input from the stop phase (DC1 stop, DC2 stop, DC3 stop, DC4 stop) is then connected via a common OR gate to an associated AND gate, the other input of which is the random-dependent signal (RNC) input, to the position counter, the position counter is connected to the 5 Bit address registers associated with the individual indicator means, said registers being connected via bi-stable multi vibrators and corresponding AND gates and inverters to control signals (DC10, DC20, DC30, DC40) which are formed by linking the signals for driving the individual indicator means during the predetermined operating time and the signals for driving the individual indicator means during the operating time determined by the random number generator and the 5 Bit address registers are connected to a programmed matrix by way of code convertors and 1 out of 16 decoders.

The advantages achieved in accordance with the present invention reside more particularly in the feature that the circuit is flexible and, due to its design, not limited in the number of winning combinations. In addition it has no mechanical contacts thus ensuring a high degree of reliability and, moreover, it can serve equally well as the starting point for a remote indicating system. The apparatus itself is simple and operates within a very short period, i.e., the entire process is electronic, the indicator means carrying a plurality of game symbols only fulfilling the function of an indicating unit.

The present invention will be described further, by way of example, with reference to the accompanying drawings, in which: —

Fig. 1 shows a first embodiment of a circuit for carrying out the method of the present invention in which the individual indicator means are each driven by a stepping motor; and

Fig. 2 shows a second embodiment of a circuit according to the invention, in which the indicator means are driven by means of a common motor.

According to Fig. 1, a photo transistor 2 having an attached amplifier 3, is associated with an indicator means 1. A zero position indicator 4 is present on the indicator means 1 so that the zero position can be scanned by the photo transistor 2. The driving motor for the indicator means 1 is a stepping motor 5 driven by pulses 6 from a pulse generator (not shown), via the OR gate 7 and the amplifier 8. The OR gate 7 is open as long as a control signal DC10 is present at the OR gate 7 via an inverter 9. The control signal DC10 is produced by a circuit (not shown) which provides a drive signal for each individual stepping motor, this drive signal for the stepping motor is connected during a predetermined operating time determined by the random number generator. At the end of the operating time, predetermined by the gaming system, a stop phase is produced which can be initiated either manually or automatically. The signal DC1 Stop opens the AND gate 10, so that the signal from the zero position indicator 4, detected by the photo-transistor 2 and amplifier 3, and filtered by the action of the filter stage 11 then resets the position counter 13 through the reset input 14 via the OR gate 12. Thus the position counter 13 operates synchronously with the indicator means 1. During the time in which the random number is not equal to zero, a number is fed into the position counter 13 and this corresponds to the position of the indicator means 1. If the externally produced random number is equal to zero, then a random-dependent signal RNC equals 1 and the control signal DC10 becomes 0, thus the stepping motor 5 is braked at that moment. The signal RNC ensures that no further signal passes through the AND gate 16, to the position counter 13. Thus the number in the position counter corresponds to the position of the indicator means 1 related to the zero position. By means of the negative going edge of the DC10 signal, the bistable multi-vibrator 17 is set so that a "1" appears at its output 18 and opens the AND gate 19, whereby the contents of the position counter 13 are fed into a 5 Bit address register 20. The bistable multi-vibrator is then reset by an externally produced reset operating signal γ so that a "0" appears at its output 18, whereby the AND gate 19 is blocked, and the address register 20 is switched to cyclic operation via the inverter 21. The slide command is given to the position counter 13 and the 5 Bit address register 20 by the clock signal ϕ_1/ϕ_2. The outputs of the 5 Bit address register 20 are connected to a code converter 22. In the code converter 22 the 5 Bit signal is changed to a 4 Bit signal. The outputs of the code converter 22 lead to a 1 out of 16 decoder 23. The outputs of the 1 of 16 decoder 23 are coupled in a matrix 24 to prize outputs 25.

The above-described cycle of the indicator means 1 is repeated with the other indicator means 26, 27, 28. Associated with the indicator means 26 are the photo-transistor 29, the amplifier 30 and the AND gate 31, associated with the indicator means 27 are the photo transistor 32, the amplifier 33 and the AND gate 34, and associated with the indicator means 28 are the photo-transistor 35, the amplifier 36 and the AND gate

37. The AND gates 31, 34, 37 are connected to the filter stage 11. The third input of the AND gates 31, 34, 37 is the particular phase DC2 stop, DC3 stop or DC4 stop associated with the indicator means 26, 27 and 28 respectively. According to which indicator means 26, 27, 28 is now stopped, the position counter 13 is reset via the corresponding AND gate 31, 34, 37 and the OR gate 12 via the reset input 14.

If this resetting of the position counter 13 is effected for example on account of the initiation of the phase DC2 stop, then dependent on the random number a control signal DC20 through the inverter 38 and the OR gate 39 is blocked, and the stepping motor 41 previously running with the pulse 6 by way of the amplifier 40 is stopped. A number corresponding to the position of the indicator means 26 is fed to the position counter 13 by means of the pulse 6 through the AND gate 16 synchronously with the position of the indicator means 26. This operation is completed when the signal DC20 is zero and the signal RNC is 1. The bistable multivibrator 42 is now set by the negative-going edge of the signal DC20 so that its output 43 becomes "1". Thus the AND gate 44 is opened for feeding the contents of the position counter 13 into the 5 Bit address register 45. Recording in the 5 Bit address is effected by means of the clock signal ϕ_1/ϕ_2. After the contents of the position counter 13 are recorded in the 5 Bit address register 45, the bistable multivibrator 42 is reset by the external reset signal γ so that the AND gate 44 is closed and the 5 Bit address register 45 is switched to cyclic operation by way of the inverter 46. A code converter 45 with a 1 out of 16 decoder 48 is associated with this 5 Bit address register 45. The signal decoded through these stages is fed into the matrix 24.

If, therefore, the indicator means 27 or 28, for example is stopped because of the phase DC3—stop or the phase DC4 stop, the preceding operation is repeated by means of the circuit consisting of the components 49, 50, 51, 52, 53, 54, 55, 56, 57, 58 or by means of the circuit consisting of the components 59, 60, 61, 62, 63, 64, 65, 66, 67, 68.

The signals at the outputs of the decoders 23, 48, 58, 68 are combined in the matrix 24 into definite combinations so that output signals appear at one or more of the outputs 25, some of which outputs are associated with the award of a prize.

The indicator means of the embodiment according to Fig. 2 are driven by a common motor. The motor drives an intermediate gear by way of two circular belts the driving force is then transmitted to three driving wheels by way of a toothed-belt. The driving wheels are the driving parts of the friction clutches for the drive of the indicator means. The components used in this embodiment, which correspond to those already described, have the same reference numerals. The indicator means 69 comprises, apart from the zero position indicator 4, also a position indicator 73 for each possible position of the indicator means. If, for example, the phase DC1 stop is initiated by an external circuit, then a signal, filtered by means of the filter stage 11, is fed through the AND gate 10 and the OR gate 12 to the return input 14 of the position counter 13 from the photo-transistor 2 and the amplifier 3. At the same time the AND gate 74 opens for the signals from the photo-transistor 75 scanning the position indicators 73 and conducted through the amplifier 76. The output of the AND gate 74 leads through the OR gate 77 to the AND gate 16. The signal RNC opens, by way of the inverter 15, the AND gate 16 for the signals coming from the OR gate 77 until the externally produced random number is equal to zero, and the signal RNC is equal to one, and the signal DC10 is equal to zero. Thus by means of the signal DC10 and a circuit (not shown), the indicator means 69 is stopped. The content of the position counter 13 now corresponds to the position of the indicator means 69 relative to the zero position. The bistable multivibrator 17 is now set by the negative going edge of the signal DC10 so that a one appears at its output 18 which opens the AND gate 19, whereby the content of the position counter 13 is fed into the 5 Bit address register 20. After this operation the bistable multivibrator 17 is reset by an externally produced operating signal γ so that a zero appears at its output 18, whereby the AND gate 19 is blocked and the 5 Bit address register 20 is controlled for cyclic operation by way of the inverter 21. The shift command is passed to the position counter 13 and the 5 Bit address register 20 by the clock signal ϕ_1/ϕ_2. The 5 Bit address register 20 is connected by its output to a code converter 22. In the code converter 22 the 5 Bit signal is converted to a 4 Bit signal. The outputs of the code converter 22 lead to a 1 out of 16 decoder 23. The outputs of the 1 out of 16 decoder 23 are joined to form prize outputs 25 in a prize matrix 24.

The above described cycle of the indicator means 69 is repeated with the other indicator means 70, 71, 72. Associated with the indicator means 70 is the photo-transistor 29, the amplifier 30 and the gate 31; associated with the indicator means 71 is the photo-transistor 32, the amplifier 33 and the AND gate 34 and associated with the

indicator means 72 is the photo-transistor 35, the amplifier 36 and the AND gate 37. Furthermore, the indicator means 70 is connected via the photo-transistor 78, the amplifier 84 and the AND gate 81, the indicator means 71 is connected via the photo-transistor 79 the amplifier 85 and the AND gate 82, and the indicator means 72 is connected via the photo-transistor 80, the amplifier 86 and the AND gate 83 to the OR gate 77.

The AND gates 31, 34, 37 are coupled to the filter stage 11. The third input of the AND gates 31, 34, 37 and the second inputs of the AND gates 81, 82, 83 are the particular phase DC2 stop, DC3 stop and DC4 stop associated with the respective indicator means 70, 71, 72. According to which indicator means 70, 71, 72, is now stopped, the position counter 13 is reset via the corresponding AND gate 31, 34, 37 and the OR gate 12 via the return input 14. The process is continued according to that of the preceding embodiment so that, in turn, the signals on the outputs of the decoders 23, 48, 58, 68 are combined in the matrix 24 into definite combinations, whereby, if desired, one or more prize outputs 25 are actuated.

The two photo-transistors associated with the particular indicator means are preferably replaced functionally by a single photo-transistor, due to the fact that a predetermined length may be given to the position pulses and a length differing from this length may be given to the zero position, and the particular position may then be obtained from the time ratio of these pulses to each other by means of a cnventional gate circuit.

The circuits are preferably designed in the MOS integrated circuit technique.

WHAT WE CLAIM IS: —

1. Apparatus for producing and identifying winning combinations for a gaming apparatus, comprising a random number generator for producing random operating pulses for determining the positions of a plurality of indicator means of the gaming apparatus and for providing a count, on a position counter corresponding to the positions of the indicator means, a preprogrammed matrix connected to the counter via an encoder and a decoder, for identifying whether there is a winning combination associated with the count corresponding to the positions of the indicator means.

2. Apparatus as claimed in claim 1 in which each indicator means has a zero position indicator and an associated photo-transistor detector, which photo-transistors are connected to the position counter via a respective AND gate controlled by a respective stop phase, and a common OR gate; each indicator means being driven by a stepping motor controlled by a control signal which connects a drive signal for driving each individual stepping motor during a predetermined operating time determined by the random number generator, and a signal dependent on the value of the random number is coupled to the position counter the output of which is connected to address registers which are associated with the individual indicator means and are attached via code convertors and 1 out of 16 decoders to the programmed matrix.

3. Apparatus as claimed in claim 2, in which each stepping motor is driven by means of a common pulse via an OR gate and an amplifier.

4. Apparatus as claimed in claims 2 and 3 in which each OR gate is connected by an inverter to each control signal input.

5. Apparatus as claimed in claims 2-4, in which the random-dependent signal is connected by an inverter and an AND gate to the position counter.

6. Apparatus as claimed in any one of claims 2-5, in which the position counter is connected by way of AND gates to 5 Bit address registers each AND gate having an input from a bi-stable multi-vibrator the state of which is determined by the control signal input and an external operating signal input, and an inverter is interposed in a connection between the bi-stable multi-vibrators and the 5 Bit address registers.

7. Apparatus as claimed in claim 1 in which each indicator means is driven by a common motor via friction clutches, each indicator means having a zero position indicator with an associated photo-transistor the output of which photo-transistor is connected to one input of an AND gate, another input coming from a stop phase, the AND gate is coupled via a common OR gate to the position counter, furthermore, each indicator means has a position indicator for each position of the indicator means and has an associated photo-transistor the output of which is connected to an AND gate which has another input from the stop phase and is then connected via a common OR gate to an associated AND gate, the other input of which is a random-dependent signal input, to the position counter, the position counter is connected to the 5 Bit address registers associated with the individual indicator means, said registers being connected to respective bi-stable multi-vibrators, AND gates and inverters, controlled by control signals which also control the connection of the signals for driving the individual indicator means during the predetermined operating time determined by the random number generator and the 5 Bit address registers are connected to a programmed

matrix by way of code converters and 1 out 16 decoders.

8. Apparatus as claimed in claims 2-7, in which the circuit is designed as an integrated circuit.

9. Apparatus for producing and identifying winning combinations for a gaming apparatus substantially as herein described with reference to and as illustrated in Fig. 1 of the accompanying drawings.

10. Apparatus for producing and identifying winning combinations for a gaming apparatus substantially as herein described with reference to and as illustrated in Fig. 2 of the accompanying drawings.

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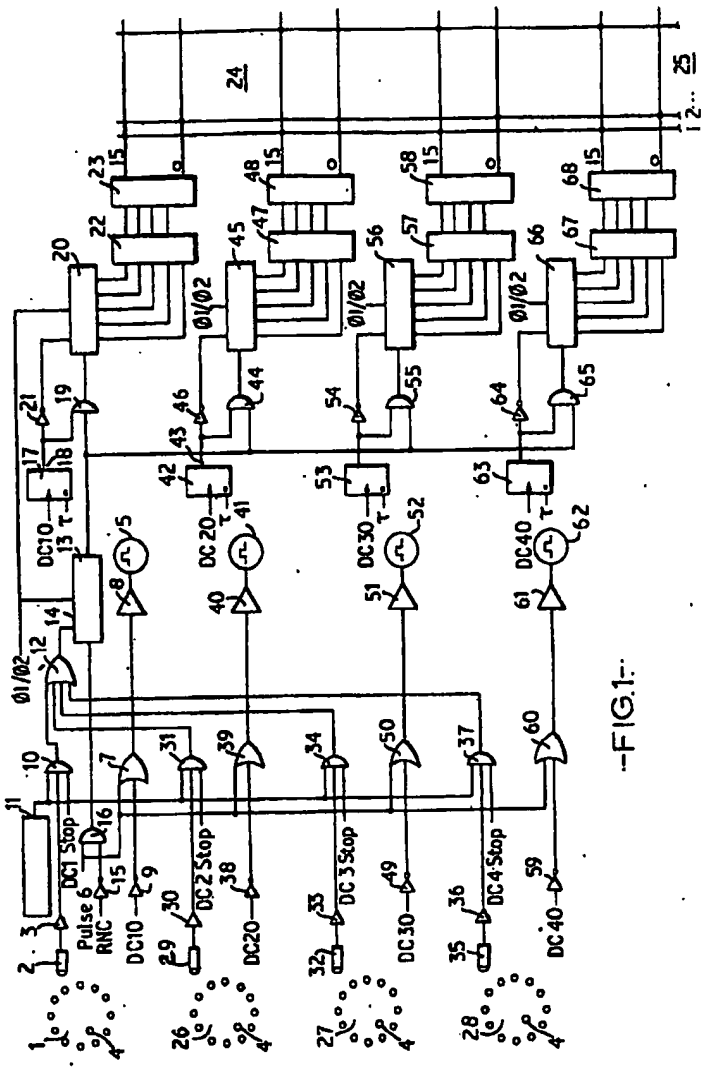

FIG.1.

1430007 COMPLETE SPECIFICATION
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Sheet 2

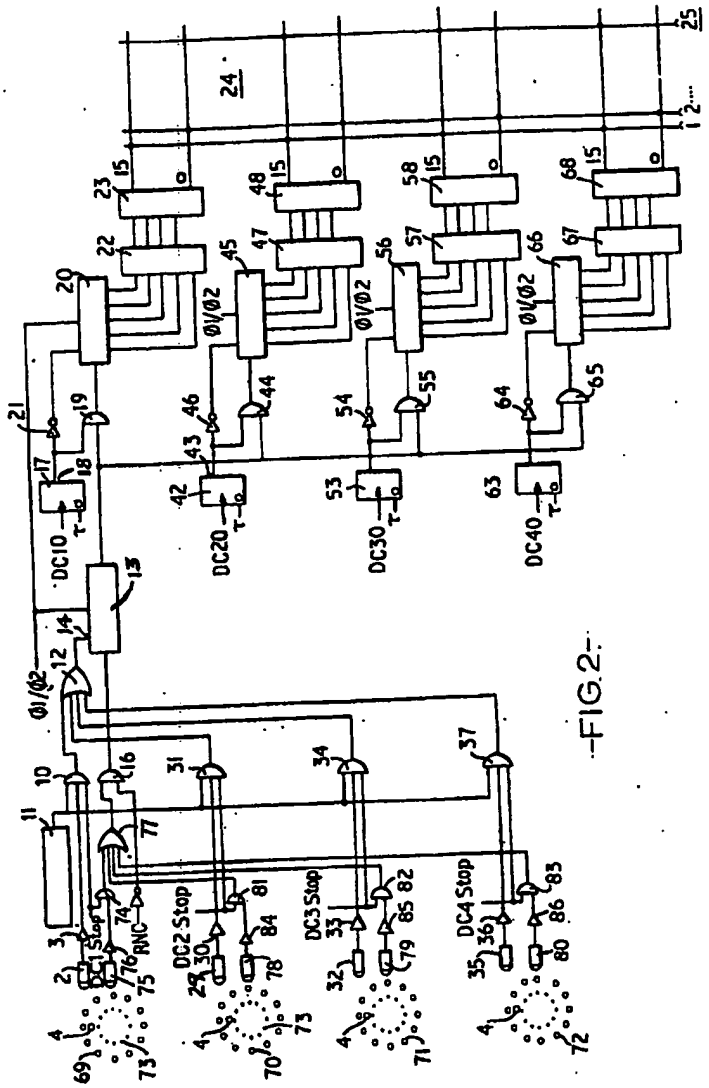

FIG.2